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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/243,101	02/02/1999	JOSHUA B. SUSSER	08993/007001	2006

7590 01/23/2003

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EXAMINER
VU, TUAN A

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 01/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Continuation of Attachment(s) 6). Other: IDS (PTO-1449) Paper No(s) 11,12,13.

Office Action Summary	Application No. 09/243,101	Applicant(s) SUSSER ET AL.	
	Examiner Tuan A Vu	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/02/1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7,8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet* .

DETAILED ACTION

1. This action is responsive to the application filed February 2, 1999, and IDS submitted 10/16/2000, 01/09/2002, 6/19/2002, 10/28/2002, and 12/16/2002.

Claims 1-58 have been submitted for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-3, 9-11, 13, 15-16, 22-24, and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The act recited as "the program can be loaded to and executed by ... fewer than 32 bits", lines 4-6, is not performed by any element recited in the structural combination laid out in the first part of the claim, lines 1-3, i.e. there is omission of a cooperative structure in enabling the previously recited elements, e.g. software program (lines 1-3), to perform the step/action described in lines 4-6.

Likewise, claims 2, 3, 9-11, the limitation following the term "wherein" depicts an act being performed but which is not structurally and cooperatively connected to the elements recited in the base claim 1 for the same indefiniteness mentioned above.

Claims 15 and 16 are also rejected for the same indefiniteness as mentioned respectively, in claim1 and claims 2-13, listed above.

Claims 1-3, 9-11, 13, 15-16, 22-24, and 26 are rejected to because of the following indefiniteness: the term "can be" used to limit an action, e.g. "wherein the instructions can be executed", e.g. line 2 claim 1, fails to clearly specify if a limitation is or is not. Such usage of term "can be" is repeated once among the above claims. The examiner will interpret and treat this term as if it were – operable in being -- or -- are --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> Note: 35 U.S.C. § 102(e), as revised by the AIPA and H.R. 2215, applies to all qualifying references, except when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. For such patents, the prior art date is determined under 35 U.S.C. § 102(e) as it existed prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. § 102(e)).

5. Claims 1, 3-5, 9-11, 13-15, 16-18, 22, 23, 24, 26-29, 31, 32, 36-40, 42, 43, 45-48, 52-55, and 58 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilkinson et al., USPN: 6,308,317 (hereinafter Wilkinson).

As per claim 1, Wilkinson discloses an application software program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18 – Note: stack parameters checking is equivalent to type and reference safe checking prior to instructions execution) residing on a computer-readable medium (*Loadable application A, B,*

Fig. 14); wherein the program can be loaded to and executed (*Loading and Execution control 120*, Fig. 14) by a *Integrated Circuit Card*, i.e. resource-constrained device as claimed (hereinafter RCD) that is based on a processor architecture of fewer than 32 bits (Fig. 1, 13; col. 7, lines 43-56).

As per claim 3, Wilkinson further discloses that the program of claim 1 can be executed by a resource-constrained device based on a 8-bit architecture (col. 7, lines 43-56).

As per claim 4, Wilkinson further discloses an 8-bit operation code (col. 7, lines 43-56).

As per claim 5, Wilkinson further discloses a hardware platform-independent sequence of instructions (*byte code* – Fig. 5, 6, 11, 17).

As per claims 9 and 10, Wilkinson further discloses a virtual machine (re claim 9) running on a microprocessor residing on the resource-constrained device (col. 1, lines 16-34; *Integrated Circuit Card, JVM 16* -- Fig. 1); and a (re claim 10) portable smart card (*smart card 210* -- Fig. 21, 22).

As per claim 11, Wilkinson further discloses a device that supports multiple data types (col. 14, lines 44-49), wherein the instructions sequence includes data manipulation instructions (e.g. Fig. 7), and wherein each data manipulation instruction is specific to a particular type (col. 14, lines 54-62; Fig. 7, 8, 9,16 – Note: byte codes transformed or translated into other forms of instructions specific to a looked-up data type is equivalent to data manipulation instruction specific to a type).

As per claim 13, Wilkinson discloses data manipulation instruction associated with a data type and multiple references type (col. 14, lines 44-49), one of such reference is a class type (e.g. Fig. 9) among other types.

As per claim 14, Wilkinson discloses one composite instruction for performing an operation on a current object (e.g. *ILOAD_0, ILOAD_1*, Fig; 7 – Note: instruction ILOAD, object = 0, 1).

As per claim 15, Wilkinson discloses an application software program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18 – Note: stack parameters checking is equivalent to type and reference safe checking prior to instructions execution) residing on a computer-readable medium (*Loadable application A, B*, Fig. 14); wherein the program can be loaded to and executed by a *Integrated Circuit Card*, i.e. resource-constrained device as claimed (hereinafter RCD) having random access memory with a capacity of no more than 64 Kbytes (Fig. 1; col. 7, lines 43-56).

As per claim 16, Wilkinson further discloses a resource-constrained device having RAM of no more than 4Kbytes (col. 7, lines 43-56).

As per claims 17 and 18, these are claim 15 versions of claims 4 and 5 hence incorporate the same rejections set forth therein.

As per claims 22 and 23, these are claim 15 versions of respectively, claims 9 and 10 above; hence incorporate the same rejections set forth therein.

As per claim 24, this is claim 15 version of claim 11 above, hence incorporates the same rejection set forth therein.

As per claims 26 and 27, these are claim 15 versions of respectively, claims 13 and 14 above; hence incorporate the same rejections set forth therein.

As per claim 28, Wilkinson discloses a resource-constrained device (Fig. 2) comprising:

a memory for storing (e.g. *Card ROM 140* -- Fig. 14) an application program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18);

a random access memory having capacity of no more than about 64 Kbytes (col. 7, lines 43-56); and

a virtual machine implemented on a microprocessor (col. 1, lines 16-34; Fig. 1,18) wherein the virtual machine is capable of executing the sequence of instructions (*Loading and Execution control 120*, Fig. 14).

As per claims 29, 31, and 32 these are claim 28 versions of respectively, claims 3, 4, and 5 above, hence incorporate the respective rejections set forth therein.

As per claims 36 and 37, these are claim 28 versions of respectively, claims 11 and 14 above, hence incorporate the respective rejections set forth therein.

As per claim 38, Wilkinson discloses a resource-constrained device (Fig. 2) comprising:

a memory for storing (e.g. *Card ROM 140* -- Fig. 14) an application program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18); and

a virtual machine implemented on a microprocessor (col. 1, lines 16-34; Fig. 1,18) that is based on an architecture of less than 32 bits (col. 7, lines 43-56), wherein the virtual machine is capable of executing the sequence of instructions (*Loading and Execution control 120*, Fig. 14).

As per claim 39, Wilkinson discloses a resource-constrained device (Fig. 2) comprising: memory for storing (e.g. *Card ROM 140* -- Fig. 14) an application program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12,

18); a random access memory having capacity of no more than about 64 Kbytes (col. 7, lines 43-56); and a processor capable of executing the sequence of instructions (col. 1, lines 16-34; Fig. 1,18).

As per claim 40, this is claim 39 version of claim 3 above hence incorporates the same rejection set forth therein.

As per claim 42, Wilkinson discloses a resource-constrained device (Fig. 2) comprising: memory for storing (e.g. *Card ROM 140* -- Fig. 14) an application program comprising an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18); a random access memory having capacity of no more than about 64 Kbytes (col. 7, lines 43-56); and an application-specific integrated circuit (ASIC) capable of executing the sequence of instructions (col. 3, lines 17-24; Fig. 1; *Loading and Execution control 120*, Fig. 14).

As per claim 43, this is claim 42 version of claim 3 above hence incorporates the same rejection set forth therein.

As per claim 45, this claim is similar to claim 28 above, hence incorporates the same corresponding rejections therein, except that the resource-constrained device (RCD) therein is herein a smart card; which limitation is also disclosed by Wilkinson (e.g. *smart card 210* -- Fig. 21, 22).

As per claim 46, Wilkinson further discloses a Java card virtual machine (*Card JVM 16*, Fig. 1).

As per claims 47 and 48, these are claim 45 versions of respectively, claims 4 and 5 above, hence incorporate the respective rejections set forth therein.

As per claims 52 and 53, these are claim 45 versions of respectively, claims 11 and 14 above, hence incorporate the respective rejections set forth therein.

As per claim 54, Wilkinson discloses a method using an application software program including an object-oriented, verifiable, type-safe and pointer-safe sequence of instructions (e.g. Fig. 5, 12, 18), the method comprising: receiving (*Integrated Circuit Card 10*, Fig. 2) the software program in a resource-constrained device (RCD) having random access memory (Fig. 14; col. 7, lines 43-56) with no more than about 64Kbytes; and executing the sequence of instructions on the RCD (*Loading and Execution control 120*, Fig. 14; Fig .18).

As per claim 55, Wilkinson further discloses storing the sequence of instructions on the RCD (e.g. *Card ROM 140* -- Fig. 14).

As per claim 58, Wilkinson further discloses transforming constant pool indices in the received set of instructions to corresponding data values (col. 9, lines 25-41; Fig 5; col. 9, line 64 to col. 10, line 10).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12, 25, and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilkinson et al., USPN: 6,308,317, as applied to claims 11, 24, and 55 above.

As per claim 12, Wilkinson discloses data manipulation instruction associated with a data type but does not specify that such data manipulation instruction is selected from a 8-bit, 16-

bit, or 32-bit signed two's complement integer numeric type. However, Wilkinson suggests the possibility of operating with 8,16 or 32-bit microprocessor (col. 1, line 61 to col. 2, line 2) and operation in the RCD being performed on 16-bit integers (col. 9, lines 29-41). One of ordinary skill in the art at the time of the invention would recognize the need for implementing a two's complement integer numeric type for each appropriate set of processor able to handle either 8, 16 or 32 bit processor as suggested by Wilkinson; and that official notice is taken that implementing 8-to-32 bit 2's complement integer type architecture is a well-known concept in the art of building processor. Hence, it would have been obvious for an ordinary skill in the art at the time of the invention was made, to implement a 8 or 16 or 32 two's complement integer numeric type instruction set to Wilkinson's small device (RCD) application building system because that would enable the RCD to perform more advanced, larger numerical data-intensive, or complicated type of instructions in the software applications needed in today's technology and also to ensure the cross-platform portability of the product.

As per claim 25, in reference to claim 24, this claim recites the same limitations in claim 12 above, hence incorporates the same rejection as set forth therein.

As per claims 56 and 57, Wilkinson further suggests retrieving security-related data over a communication network and the Internet (col. 3, lines 40-46); and discloses downloading of software onto the RDC (Fig. 1, 2; col. 3, line 60 to col. 4, line 8; col. 7, line 66 to col. 8, line 8); **but does not explicitly teach** accessing the software program to download onto the RDC from the a network (re claim 56) or Internet (re claim 57). Official notice is taken that accessing and distributing software and application data over a network or Internet is a well-known concept in computer communication and networking. Thus, it would have been obvious for one of ordinary

skill in the art at the time the invention was made to add to Wilkinson's system the accessing of application programs over the Internet or network because this would improve the availability of program to load the RCD while enhancing the resource usage efficiency for not overburdening the storage of the host machine and the RCD connected to it.

8. Claims 2, 6-8, 19-21, 30, 33-35, 41, 44, 49, 50, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilkinson et al., USPN: 6,308,317, as applied to claim 1, 15, 28, 39, 42, 45 above, in view of Benaloh et al., USPN: 5,724, 279 (hereinafter Benaloh).

As per claim 2, in reference to claim 1 above, Wilkinson discloses an application program downloadable into a resource-constrained device (Fig. 1,13); **but does not explicitly disclose** that such resource-constrained device (RCD) is capable of being executing such program based on a 16-bit processor architecture. However, Wilkinson suggests the possibility of having a 16-bit microprocessor (col. 1, line 61 to col. 2, line 2) and operation in the RCD being performed on 16-bit integers (col. 9, lines 29-41). Benaloh, in a method for reducing instructions in application program modules for use on devices analogous to the RCD or *integrated circuit card* of Wilkinson, reveals the existence of 16-bit smartcards (col. 18, line 60 to col. 19, line 8). In view of Wilkinson's suggestion of a possibility for code execution based on a 16-bit architecture and the teachings of Benaloh, it would be obvious for one of ordinary skill in the art, at the time of the invention, to implement the 16-bit architecture as suggested by Wilkinson and taught by Benaloh, to the resource-constrained device (RCD) as taught by Wilkinson because this would enable the RCD to perform more advanced, data-extensive, complicated type of software applications needed in today's technology.

As per claim 6, Wilkinson further discloses that the program instructions are converted from one Java class file; and that some references to a constant pool were transformed to a form of byte code instructions suitable for reduced code space requirements (col. 10, lines 30-47; Fig. 5,6); but **fails to disclose explicitly** that the references are transformed to inline data. Benaloh, in a method for reducing instructions in application program modules for use on devices analogous to the RCD or *integrated circuit card* of Wilkinson, reveals the reduction to in-lined instructions (col. 18, line 60 to col. 19, line 8). It would be obvious for one of ordinary skill in the art, at the time of the invention, to combine the inline technique as taught by Benaloh with the class file transformation and constant pool references techniques for reducing the RCD space usage as suggested in Wilkinson because this would reduce the memory resource usage and overhead in functions call, and thus ensuring a better optimization in that a certain or established size can be efficiently handled by a resource-constrained processor such as a smart card mentioned in Benolah's above teachings.

As per claims 7 and 8, Wilkinson further discloses in the instructions of claim 6 that some references to the constant pool are transformed into (re claim 7) operands (Fig. 8,9; col. 10, lines 52-65) and into (re claim 8) operation codes in those instructions (*LDC, BIPUSH*, Fig. 7, 8); **but fails to disclose** the transformation into inline operands or operation codes. This last limitation has been addressed in claim 6 above, hence would have been obvious by virtue of the same rejection set forth therein.

As per claim 19, with reference to claim 15 above, this claim recites the same limitations in claim 6 above; hence incorporates the same rejection set forth therein.

As per claims 20 and 21, these are similar to respectively, claims 7 and 8 above, hence incorporate the same corresponding rejections set forth therein.

As per claim 30, this is claim 28 version of claim 2 above, hence incorporates the same rejection as set forth therein.

As per claims 33-35, these are claim 28 versions of respectively, claims 6-8 above, hence incorporate the respective rejections set forth therein.

As per claim 41, in reference to claim 39, this claim includes the limitation addressed in claim 2 above, hence incorporates the same rejection as set forth therein.

As per claim 44, in reference to claim 42, this claim includes the limitation addressed in claim 2 above hence incorporates the same rejection set forth therein.

As per claim 49, this is claim 45 version of claim 6 above hence incorporates the same rejection set forth therein.

As per claims 50 and 51, in reference to claim 45, these claims include the same limitations addressed in respectively, claims 7 and 8 above hence incorporates the same corresponding rejections set forth therein.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat No. 5,999,731 to Yellin et al., disclosing data type checks from byte codes.

U.S. Pat No. 6,233,683 to Chan et al., disclosing security check on smart cards issuing.

U.S. Pub No. 2001/0000814 to Montgomery et al., disclosing configuring smart cards.

U.S. Pat No. 6,332,215 to Patel et al., disclosing byte codes translation into micro-controllers.

U.S. Pat No. 5,999,732 to Bak et al., disclosing class initialization and reduction.

U.S. Pat No. 6,092,147 to Levy et al., disclosing byte code verification for smart card JVM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

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or faxed to:

(703) 746-7239, (for formal communications intended for entry)

or: (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
January 16, 2003

John Chaki
Patent Examiner